Design of a Linear Transconductance OTA using the Open Sky130 Process Design Kit

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***Abstract*—This paper describes the design, layout and simulation of a linear transconductance Operational Transconductance Amplifier (OTA) using the SkyWater 130 nm open Process Design Kit (PDK). By using a known source degeneration technique, it is possible to either decrease and linearize the transconductance of the OTA for a wider range of input voltages, making it proper for use on Gm-C filters. Only open source tools, suited for the Sky130 PDK, were used in this design, showing the applicability to analog designs.**

***Index Terms*—OTA, linear transconductance, open PDKs, Sky130, open source tools.**

I. Introduction

The Gm-C filters can be used in a great variety of applications as, for example, in disk drive read channels [1], anti-aliasing filters [2], wireless communications [3] and even in biomedical circuits [4]. It is interesting to note that these applications spread over a wide range of frequencies. The basic building block of these filters are the Gm-C integrator, composed by an operational transconductance amplifier (OTA) and a capacitor, as described in [5].

In [6], a bank of high-order passband Gm-C filters was proposed, devised to be used in a power quality measurement system. The bank is composed by ten 16th-order passband filters with a band of 15 kHz each, ranging from 2 kHz to 150 kHz. The aim of the filter bank is to measure the supraharmonic components superimposed to the line ac voltage. In that work, all simulations were done using a simplified OTA model, composed simply by a voltage-controlled current source and an output resistance. In a later work [7], simulation results were shown for a filter bank designed at transistor level, using BSIM predictive models, available in [8]. However, the OTAs and consequently the filters were not laid out.

That design revealed the need of OTAs with transconductances with several order of magnitudes, ranging from order of 10^{-7} to 10^{-3} ampères per volts (A/V). Some techniques for obtaining low transconductance OTAs are presented in [9]. Moreover, for a power quality measurement system, it is important to keep the OTAs responses linear over a wide range of input voltages. The source-degenerating scheme can provide a linear response over a wide differential input range, and was used for the design of the OTAs in [10].

The launching of the SkyWater open process design kit (PDK) in 2020 [11] filled a lack in the design of chips, especially for undergraduate students. Supported by Google, some runs were promoted for fabrication of selected projects using the process hereafter named Sky130, which is a hybrid, 130 nm, 1.8-V CMOS process. Although the majority of projects using the Sky130 PDK are currently for digital circuits, several analog projects have already been published, as in [12] and [13]. The PDK was released for use with free and open-source tools, some of them totally adapted for the Sky130 process.

This paper describes the design of a linear transconductance OTA using the source-degeneration scheme, employing the Sky130 PDK. Only open source tools were used for simulation, layout and extraction. The objective of this work is to show a guideline for those who want to start with the PDK for analog design. Simulation results will be shown for two different source-degeneration approaches.

The work is organized as follows: in Section II, the OTA structure and the design methodology is briefly described. In Section III, the layout is commented. In Section IV, simulation results for both extracted netlists are discussed. Finally, the conclusions are presented in Section V.

II. OTA Structure

The proposed topology for the OTA is based on the source-degeneration scheme, that can linearize the OTA response and either reduce its transconductance gain, if compared to the basic OTA [10]. The circuit is depicted in Fig. 1. Each transistor of the differential pair (M_1 and M_2) is biased by currents that are replica of I_B (which flows into M_B), imposed by transistors M_3 and M_4, respectively. Two resistors R_{s1} and R_{s2} are then placed among the sources of M_1 and M_2. The choice of two resistors instead of just one has the objective of give more flexibility to the layout.

The resistors can be replaced by MOSFETs in triode region, as depicted in detail in Fig. 3b, acting as voltage-controlled resistors (in this case, with gate voltage set to V_{DD} = 1.8 V).

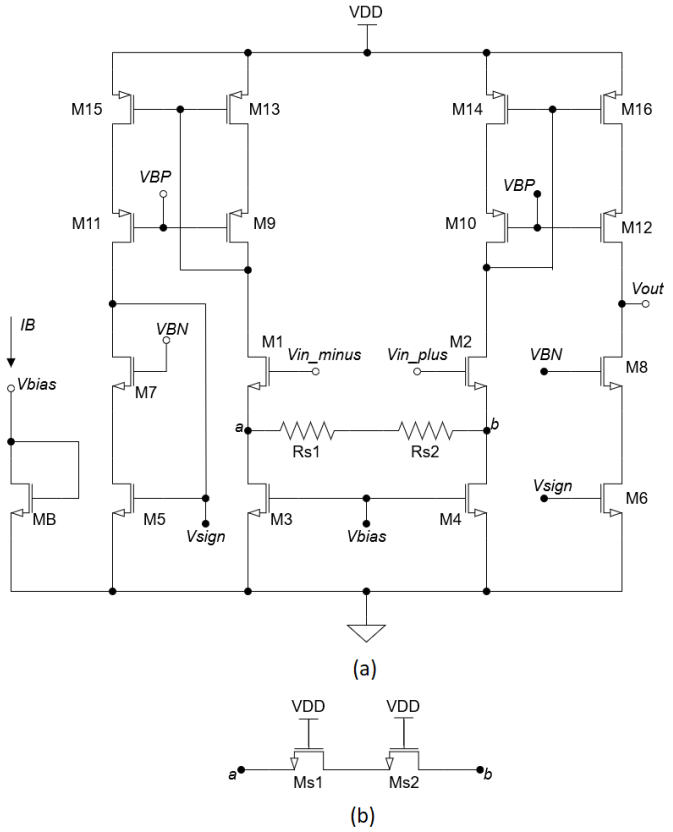

Fig. 1. OTA Sctucture. (a) Complete circuit, with source degeneration resistors; (b) Alternative source degeneration triode MOSFETs.

The MOSFETs are chosen so that their small-signal drain-source conductances, g_{ds}, are

$$g_{ds,s1} = \frac{1}{R_{s1}} \tag{1}$$

Considering that $R_{s1} = R_{s2}$, and $g_{ds,s1} = g_{ds,s2}$.

The presence of cascode stages in the circuit, properly biased at V_{BP} and V_{BN}, increase the output impedance, which is required for some filter designs. From [10], it can be demonstrated that the transconductance gain, G_m, is given by

$$G_m = \frac{g_m}{1 + g_m R_1} \tag{2}$$

Considering that g_m is the transconductance of M_1 (or M_2), given by

$$g_m = \sqrt{2k_n^{'}(\frac{W}{L})_1 I_{B1}} \tag{3}$$

Where k_n' is the process transconductance parameter, $(W/L)_1$ is the aspect ratio of M_1 and I_{B1} is the biasing current of M_1. M_1 and M_2 are identical elements, so that $g_m = g_{m1} = g_{m2}$.

TABLE I
DIMENSIONS OF THE COMPONENTS OF THE OTA.

Element(s)	Aspect ratio, W/L ($\mu m/\mu m$)
M1, M2	10.0/1.0
MB, M3, M4	5.0/1.0
M5 – M8	5.0/1.0
M9 – M16	15.0/1.0
Rs1, Rs2	0.69/13.0
Ms1, Ms2 (*)	1.0/8.5 (*)

(*) for the alternative circuit

A. Design Methodology

As a design example, the desired OTA transconductance was specified at 21 $\mu A/V$. The aspect ratios of the MOSFETs of the differential pair and the resistors could be determined by (2) and (3), by arbitrating one of the values. However, it was observed that the linearity can be obtained by a compromise between $(W/L)_1$ and $R_{s1} + R_{s2}$. Moreover, the value of the tranconductance parameter k_n' is not explicitly defined in the PDK documentation. This emphasizes the need of an initial simulation, since analytical calculations just give an initial guess about the parameters. The XSCHEM tool was used for schematic diagrams capture and setting the simulation parameters, and NGSPICE was used for simulation.

An initial operation point (.op) simulation, with investigation of the transistors parameters, is useful for the appropriate choose of the transistors aspect ratios. By using the low-threshold voltage (low-Vt) MOSFETs models for all NMOS and PMOS, for a biasing current I_B = 9.5 μA, $g_{m1} = g_{m2} =$ 163 $\mu A/V$.

The Sky130 PDK allows fixed-width poly resistors [14]. The widths available are 0.35 μm, 0.69 μm, 1.41 μm, 2.85 μm and 5.73 μm. The high resistance poly resistors (Xhigh_po) exhibit a sheet resistance of 2000 Ohms per square. Some adjusts were done after first simulations, and a high-resistance poly resistor with L = 13 μm and W = 0.69 μm was chosen for R_{s1} and R_{s2} (with a 38-kΩ resistance each). The two resistors are associated in series to give the required resistance. The reason for using two resistors in series instead of a unique resistor is to facilitate the layout.

Transistors M_B, M_3 and M_4 compose a current mirror with two identical outputs, whose input current is I_B = 9.5 μA. For the version with source degeneration MOSFETs, I_B had to be adjusted on 10 μA to give similar results. In order to give an overdrive voltage close to 110 mV, their aspect ratios were chosen to 5 μm/1 μm.

The remaining PMOS and NMOS transistors compose cascode current mirrors, arranged in order to produce an output current for a single-ended amplifier. The use of cascodes limits the output voltage swing, but gives to the OTA a high output impedance, which is an important parameter in design of low-frequency filters. The voltages V_{BP} = 952 mV and V_{BN} = 816 mV are provided by a simplified biasing circuit, not shown in Fig. 1, in order to let a maximum voltage swing at the output.

The resistors could be replaced by two n-channel MOSFETs operating in the linear (triode) region, as shown in the detail in

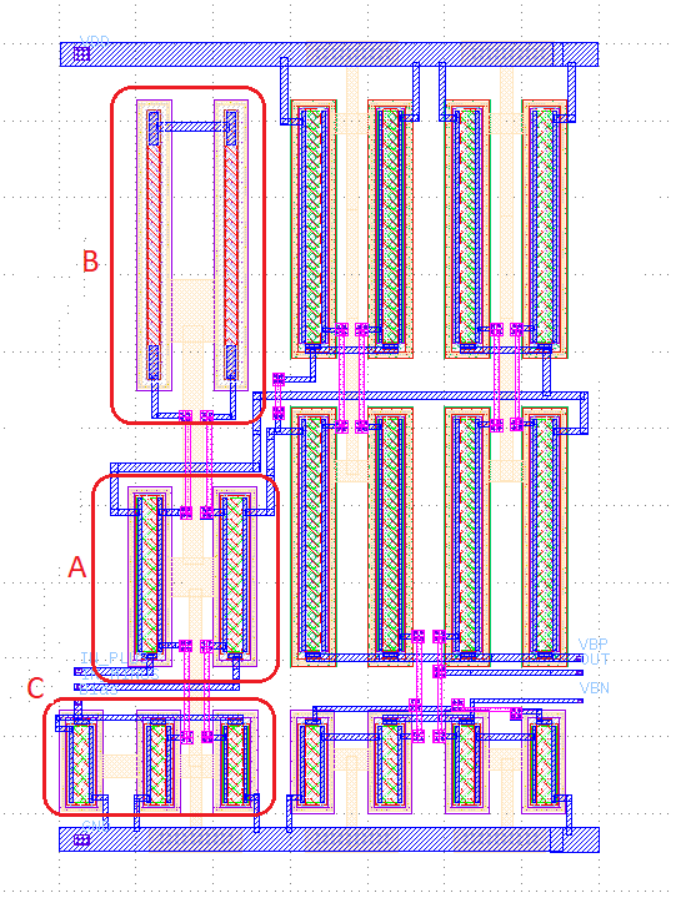

Fig. 2. OTA layout, with identification of some relevant parts: (A) differential pair; (B) source-degeneration resistors; (C) biasing transistors.

Fig. 1(b). The aspect ratios of these components were obtained after a .OP simulation, to give their conductances g_{ds} equal to $1/R_{s1,s2}$. The Table I shows all the aspect ratios (W/L) of the components.

III. Circuit Layout

The layout of the OTA was done by using two open source tools: Magic VLSI Layout Tool, an EDA software written in 1980s, re-suited for use with the Sky130 PDK; and KLayout, a more modern open source layout tool. The advantage of using Magic is the possibility of automatic generation of the circuit components (in this case, low-Vt PMOS and NMOS, and XRES poly resistors). Moreover, Magic is efficient for design rule checking (DRC) and circuit extraction.

However, considering that Magic has a poor handling interface, if compared with modern tools, the following design methodology was adopted: (i) generation of the devices in Magic, upon the dimensions contained in Table I, and exporting of the devices for GDSII format; (ii) importing of the GDSII file in KLayout, where all connections with metal layers were done; (iii) DRC in KLayout, using the package available in [15]; (iv) importing of the GDSII in Magic, for circuit extraction.

By using this strategy, it was possible to create the layout shown in Fig. 2, which emphasizes the differential pair (A), the source degeneration resistors (B) and the biasing transistors (C). The layout with source-degenerating MOSFETs has a similar aspect, just replacing the elements in (B), since the sizes of the MOSFETs occupy an area slightly lower than the high resistance resistors, for this design.

The total area of the block is 1820 μm^2 (35 μm x 52 μm). For this design, the area optimization was not prioritized, since the main objective was to test the design tools with the Sky130 PDK. The transistors and resistors, for example, were placed with individual guard rings, generated automatically by Magic, which use an additional area. For the PMOS devices, this means individual N-wells for each transistor. The metal widths and spacing between devices were also larger than the minimum allowable by the design rules.

IV. Simulation Results

The layout of Fig. 2 was extracted for post-layout simulation with the open tool NGSPICE. For evaluation of the improvement in the linearity of the source-degeneration scheme, two simulation strategies are shown: (i) the transconductance plot versus differential input voltage; (ii) a DC sweep, plotting the output current versus the differential input voltage. For comparison, results for the circuit with source-degeneration resistors are shown with results for the circuits with triode source-degeneration MOSFETs.

For all circuits, V_{DD} = 1.8 V, and V_{CM} = 0.9 V, where V_{CM} is the common-mode voltage.

For evaluating the transconductance, a step .AC analysis was applied at a fixed frequency (1 kHz), varying the DC differential voltage applied at the inputs of the differential pair, producing the plot shown in Fig. 3. It can be shown that a transconductance close to 21 $\mu A/V$ is approximately maintained over a range of about $\pm$0.59 V, evidencing the feature of the structure in obtaining a quasi-linear response for a larger range of the input signal.

The DC sweep was performed by varying the differential input voltage, resulting in the plot shown in Fig. 4. Again, it shows a practically linear response in the range of $\pm$ 0.59 V.

From the transconductance plots, it can be seen that the response for the circuit with the resistors exhibits little difference if compared with that obtained for the circuit with triode MOSFETs. However, since the g_{ds} conductances of the MOSFETs are determined by $(V_{GS} - V_t)$, where, in this case, $V_{GS} = V_{DD}$, then the sensitivity of the circuit with triode MOSFETs to supply variations is considerably higher than that obtained for the source resistors.

V. Conclusion

This paper presented the design of an OTA with linearized transconductance over a wide range of differential input voltage. It is a useful block in designing Gm-C filters.

As design example, an OTA with 21 $\mu A/V$ was considered. The source-degeneration scheme was adopted, in order to either linearize and also reduce the transconductance, which

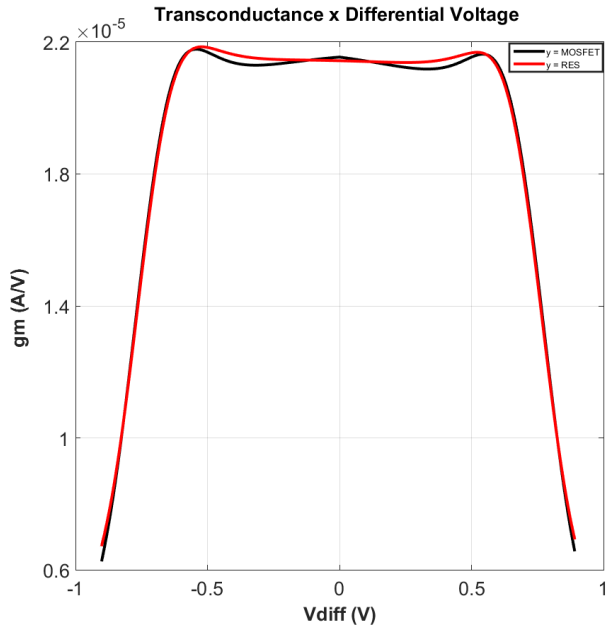

Fig. 3. Plotting of the transconductance versus input voltage, for the two approaches. Red: using resistors; Black: using triode MOSFETs.

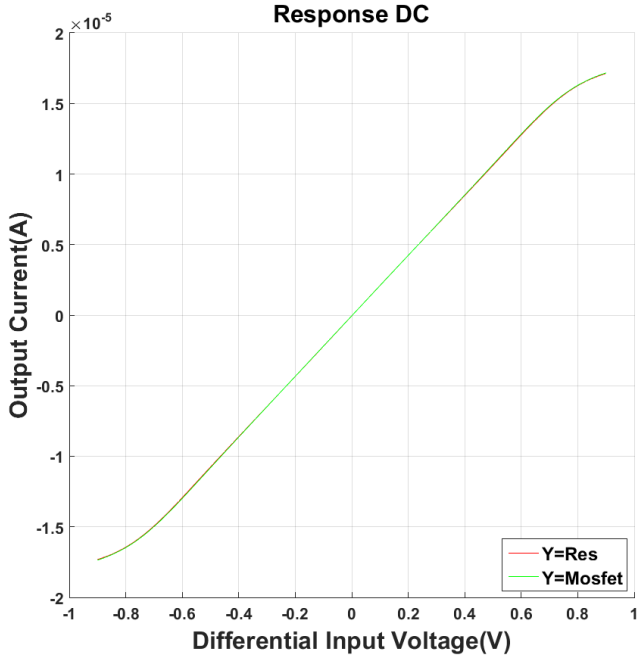

Fig. 4. Plotting of the DC sweep for the output current. Red: using resistors; Green: using triode MOSFETs.

can be important in design of low-frequency filters. However, the technique can be used in the design of linearized OTAs with transconductances of other orders of magnitude.

Although the topology itself does not present a novelty in analog circuit design, the use of the Sky130 open PDK and the employment of open source tools suited for this design kit were the differential aspects of this work.

Post-layout simulation results obtained with NGSPICE demonstrated that the purpose of achieving a linear transconductance over a wide range of input voltages was achieved, both for the circuit using resistors or using triode MOSFETs as source-degenerating elements.

The analysis of the circuit considering mismatching models of the devices is considered for future works, as well as the adaptation of this circuit to a fully differential version. In this case, a common-mode feedback circuit will be needed.

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